Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **DE**
2. **D IN**
3. **NC**
4. **R OUT**
5. **NC**
6. **GND**
7. **GND**
8. **NOT RE**
9. **RI –**
10. **RI +**
11. **DO –**
12. **DO +**
13. **VCC**
14. **VCC**

**12**

**11**

**10**

**3**

**4**

**5**

**2 1 14 13**

**6 7 8 9**

**DIE ID**

**Top Material: 95% Al / 5% Cu**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .059” X .068” DATE: 4/25/22**

**MFG: NATIONAL SEMI THICKNESS .016” P/N: DS90LV019LVDS**

**DG 10.1.2**

#### Rev B, 7/19/02